

PATENT
790001-2004



UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Hiroyuki YANO et al.
Serial No. : 09/870,085
Filed : May 30, 2001
For : MANUFACTURING METHOD OF SEMICONDUCTOR
DEVICE
Examiner : Thanhha Pham
Group Art Unit : 2813

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" Service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Edward Nay

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DECLARATION UNDER 37 C.F.R. §1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We, Hiroyuki Yano and Katsuya Okumura, declare and state that:

1. We are the co-inventors of the subject matter described and claimed in the present patent application.
2. Figures 1A, 1B and 1C of the application were mistakenly labeled as

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"Prior Art." The subject matter of figures 1A, 1B and 1C was not public knowledge at the time of filing of the Japanese priority application (JP 2000-163045, filed May 31, 2000), and was only known internally at Kabushiki Kaisha Toshiba (the assignee of the application). Accordingly, figures 1A, 1B and 1C, and the accompanying description of these figures, are not and cannot be prior art.

3. A replacement drawing sheet including figures 1A, 1B and 1C was filed concurrent with an Amendment on August 25, 2003. A copy of the replacement sheet is provided herewith. The replacement sheet amends figures 1A, 1B and 1C by deleting the designation "Prior Art." We respectfully request that the replacement drawing sheet be substituted for the corresponding previously submitted drawing sheet.

4. We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the present application or any patent issued thereon.

Date: Nov. 11, 2003

Hiroyuki Yano
Hiroyuki Yano

Date: Nov. 12, 2003

Katsuya Okumura
Katsuya Okumura

REPLACEMENT SHEET

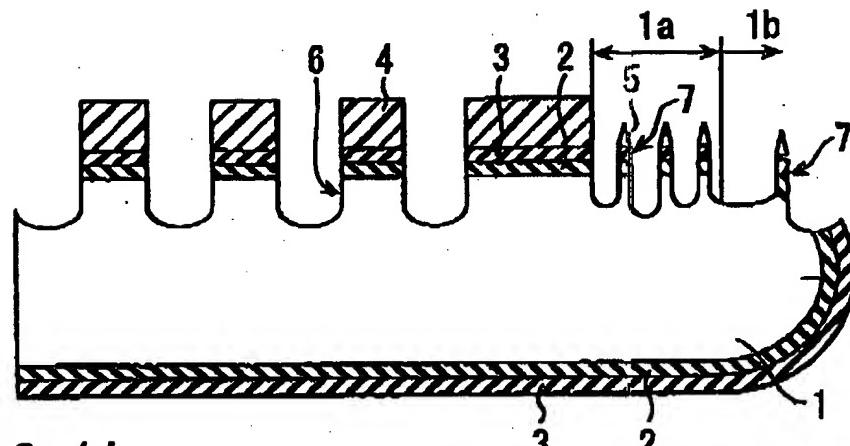


FIG. 1A

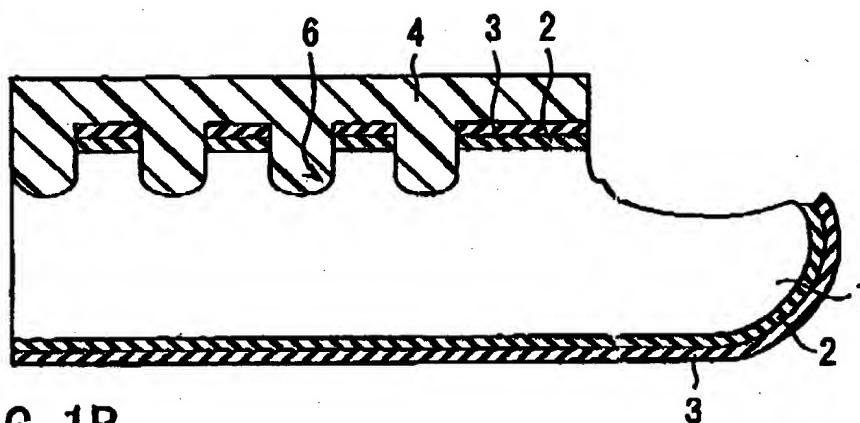


FIG. 1B

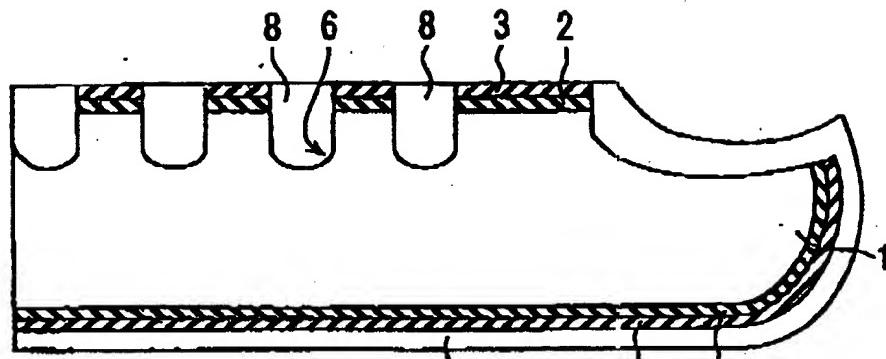


FIG. 1C